

ABSTRACT

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5 A layout method of a semiconductor device comprising the steps of: arranging active regions of a plurality of transistors having at least more than one first and second electrodes disposed on a substrate; arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning at least more than one gates having predetermined width and length at a constant gap on the substrate; and arranging a plurality of dummy gates having predetermined width and length between a plurality of transistors (or between and outside transistors) at the same gap as that of the gates

10 of transistors on the substrate, so that all the gates of transistors are arranged at a constant gap to minimize the variances in process deviations and accordingly reduce the difference of threshold voltage of transistors, thereby increasing reliability of the semiconductor device.

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